NON-VOLATILE MEMORY DEVICE HAVING SELECT TRANSISTOR STRUCTURE AND SONOS CELL STRUCTURE AND METHOD FOR FABRICATING THE DEVICE

ABSTRACT OF THE DISCLOSURE

Non-volatile memory devices according to embodiments of the invention can include, for example, a semiconductor substrate, a source region, a drain region, an impurity region, a vertical structure, a control gate insulating layer, a control gate electrode, a gate insulating layer, and a gate electrode. The impurity region is in a floating state between the source region and the drain region. The vertical structure is formed of a tunneling layer, a charge trapping layer, and a blocking layer sequentially stacked between the source region and the impurity region. The control gate insulating layer is between the source region and the impurity region and adjacent to the vertical structure. The control gate electrode is formed on the vertical structure and the control gate insulating layer. The gate insulating layer is between the impurity region and the drain region. The gate electrode is formed on the gate insulating layer.